UART Module Description Document

1. **Introduction**

The UART is divided into two functional modules: FUART and BUART.

FUART @ 96 MHz supports any baud rate from 1200 bps to 3,000,000 bps (halved when using RC 48 MHz). It supports configurable 5/6/7/8 data bits, 1 or 2 stop bits, and odd, even, or no parity. Each of its transmit and receive FIFO has a depth of 4 bytes.

BUART @ 96 MHz supports any baud rate from 1200 bps to 3,000,000 bps (halved to 600 bps–1.5 Mbps at RC 48 MHz, with possible slight deviations). It supports configurable 5/6/7/8 data bits, 1 or 2 stop bits, and odd, even, or no parity. It can use either internal or external FIFOs as independent transmit and receive buffers. The external FIFO buffer depth can be up to 12 KB.

**2. Main Features**

FUART Features:

The baud rate is dynamically configurable, supporting 1200 bps to 3 Mbps at 96 MHz and 600 bps to 1.5 Mbps at 48 MHz.

Data width: 5 to 8 bits

Stop bits supports 1 to 2 bits

 Supports parity checking

Supports frame format error check, overflow error check, and parity error check

Supports receive interrupt, transmit interrupt, and error interrupt

Supports full-duplex transmit and receive, each with an independent 4-byte FIFO

BUART Features:

Full-duplex transmit and receive

Dynamic baud rate configuration, 1200 bps to 3 Mbps @ 96 MHz, 600 bps to 1.5 Mbps @ RC48 MHz, other clocks not supported

Data width: 5 to 8 bits

 Stop bits supports 1 to 2 bits

Supports parity check (only for internal FIFO)

Supports frame format error flag, overflow error flag, and parity error flag check (only for internal FIFO)

Supports interrupt notifications for data reception, transmit buffer empty, and errors (some only for internal FIFO)

Supports independent transmit/receive FIFOs:Internal FIFO depth of 4 bytes.xternal FIFO using PMEM

Supports bidirectional flow control when using external FIFO with depth ≥ 5 bytes

**3. Functional Description**

**3.1. FUART External Physical Connection**  
Only a simple cross connection is required, supporting only basic data transmit/receive exchange without flow control. It should be noted that the device side must meet or be compatible with UART electrical specifications. For high-speed transmission, the interconnection cable should be kept short, and interference resistance is required.

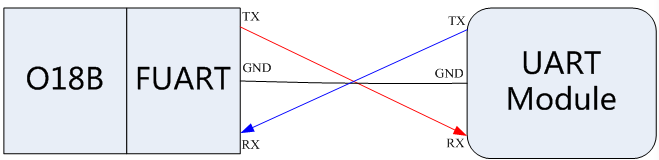
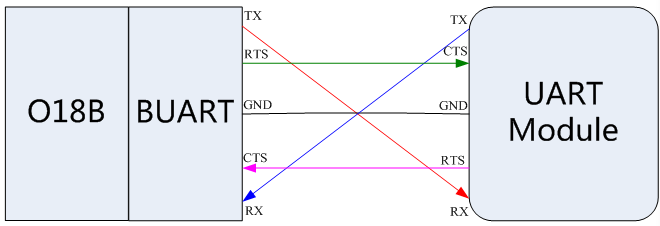


Figure 1 FUART Connection Method

**3.2 BUART External Physical Connection Method**  
A simple cross connection is sufficient to support basic transmit/receive data exchange. If flow control is required, connect RTS/CTS accordingly. Note that the device side must meet or be compatible with UART electrical specifications. For high-speed transmission, the interconnection cable should not be too long, and good anti-interference capability is required.

Figure 2 BUART Connection Method

**3.3 Comparison Between BUART and FUART**  
BUART is based on the basic functions of FUART, with the addition of external FIFO and bidirectional flow control support. In other words, BUART can also be used as a FUART.

**3.4 Driver Interfaces**  
Table 1 FUART Driver Interface Functions

|  |  |
| --- | --- |
| **Function Name** | **Description** |
| FuartInit | Initialize Fuart and set parameters |
| GpioFuartRxIoConfig | Fuart Rx pin multiplexing configuration |
| GpioFuartTxIoConfig | Fuart Tx pin multiplexing configuration |
| FuartRecv | FUART data reception |
| FuartSend | FUART data transmission |
| FuartIOctl | Set/Get various configurations of FUART |

Table 2 BUART Driver Interface Functions

|  |  |
| --- | --- |
| **Function Name** | **Description** |
| BuartInit | Initialize Buart and set parameters |
| GpioBuartRxIoConfig | Buart Rx pin multiplexing configuration |
| GpioBuartTxIoConfig | Buart Tx pin multiplexing configuration |
| GpioBuartCtsIoConfig | Buart Cts pin multiplexing configuration |
| GpioBuartRtsIoConfig | Buart Rts pin multiplexing configuration |
| BuartRecv | BUART data reception |
| BuartSend | BUART data transmission |
| BuartIOctl | Set/Get various configurations of BUART |
| BuartExFifoInit | Set external FIFO |

**4. Usage Process**

**4.1 FUART Initialization Process:**

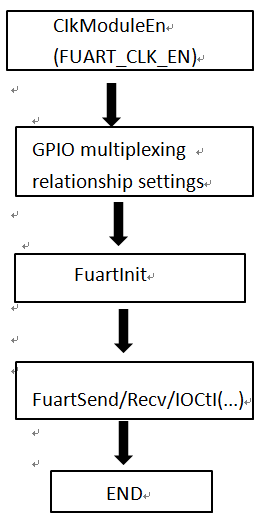
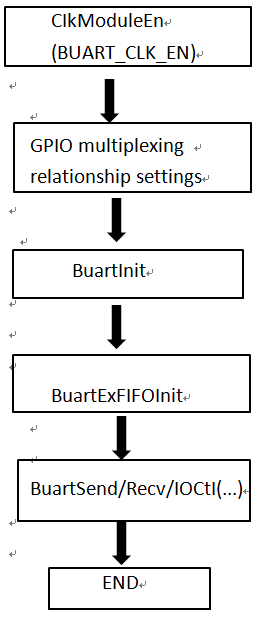


Figure 3 FUART Module Initialization Flow

**4.2 BUART Initialization Process:**

  
Figure 4 BUART Module Initialization Flow

**5. UART Baud Rate Accuracy Description**  
Different baud rates require different register settings, which are already encapsulated in the library. Different baud rates also have different theoretical errors.

When the system clock fclk is 96 MHz and the required baud rate is x, the baud\_clk frequency should be eight times x. The baud\_clk frequency is obtained from the divided clock of fclk. For example, if the desired baud rate is 1,382,400, then fclk divided by 8x equals 8.68, so clk\_div should be set to 7 and clk\_div\_frac should be set to 5.

The following tables show the typical parameter configurations for common baud rates and the allowable clock frequency deviation. “+” indicates higher (faster) than the standard frequency, and “–” indicates lower (slower) than the standard frequency.

Table 3 Typical Baud Rate Tolerance Table when the System Clock is 96 MHz

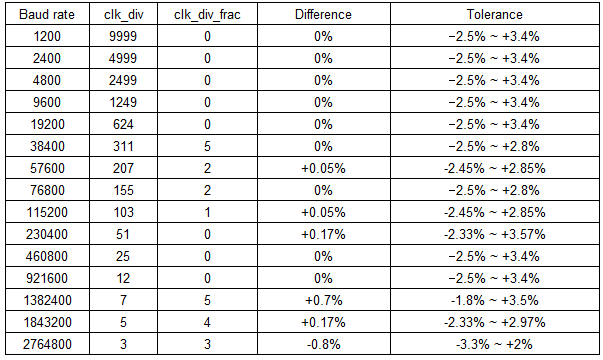
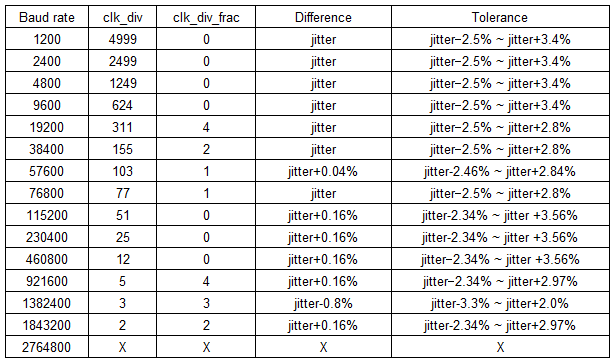


Table 4 Typical Baud Rate Tolerance Table when the System Clock is 48 MHz



In these tables:jitter represents the jitter of the RC48M clock.X indicates that this baud rate is not applicable under RC48M